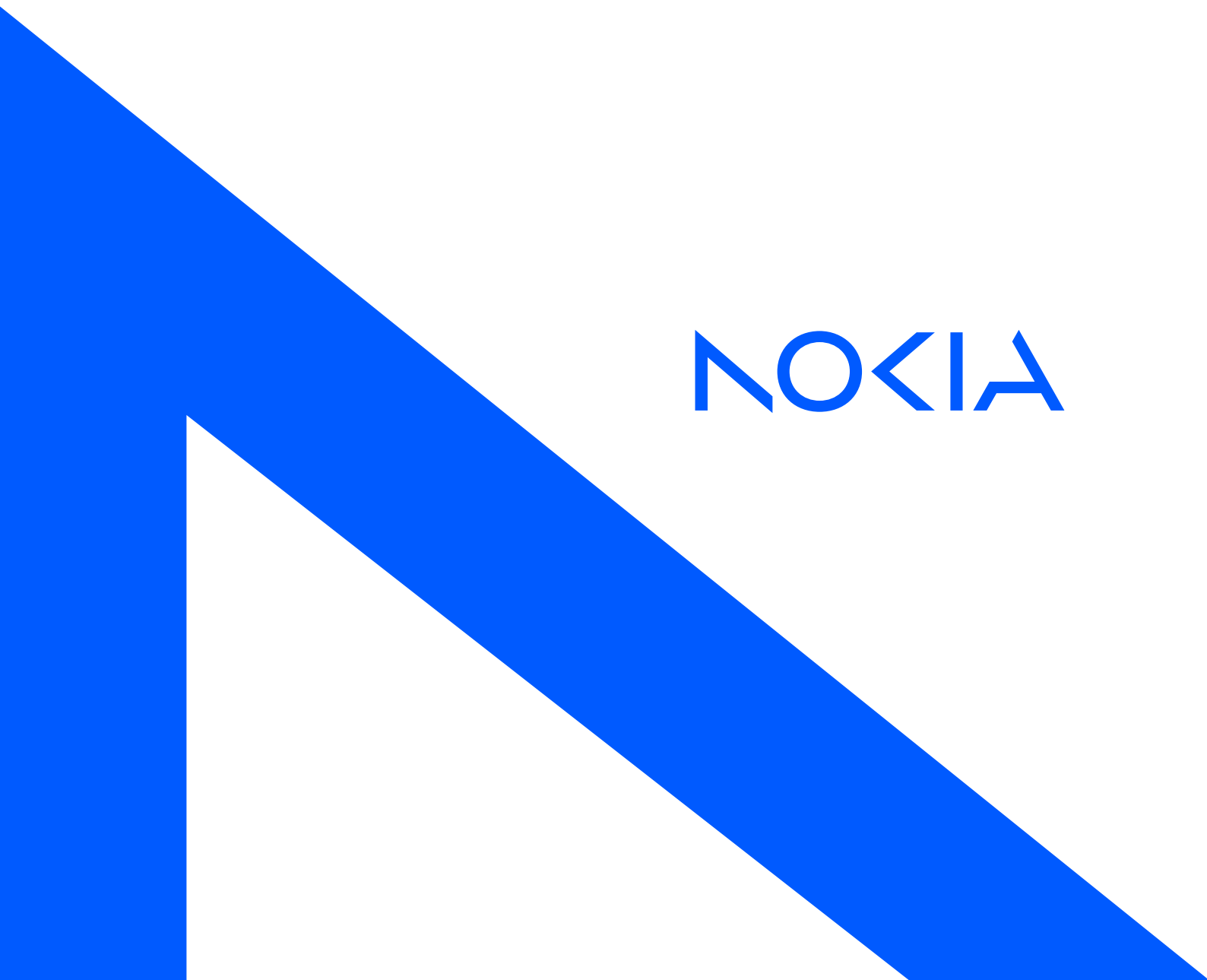
Nokia FP5 silicon innovation

The new route to remarkable in IP networking

Application note



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IP networks today

Today's networking environment is full of uncertainty. We've seen tremendous changes in the ways we work, shop, go to school and communicate. The role of networking has never been so critical to our everyday lives. Transitioning out of the COVID era, networks deployed globally needed to adapt to this "new normal" while continuing to sustain the traffic they carried before the world changed.

The ongoing challenges our IP networks face shows us not only the positive impacts of IP networks on our day-to-day lives but also their potential to drive new business models and to adapt as the world evolves. The agility, network security and sustainability built into networks are not just nice-to-haves; they are mandatory requirements for the continued success of IP networking.

Market initiatives including 5G, the internet of things (IoT), smart grids, smart cities and the age of digital transformation are all rising in parallel with those change-driven network demands. Maintaining growth, coping with new network expansion and providing the best user experience while maximizing network resources can be a daunting task. This, however, is the goal of capable platforms while delivering the highest return on investment.

The new route to remarkable in IP networking

With the right structural elements, IP networks can scale without limits and adapt to address new opportunities. Breakthrough silicon innovation from Nokia has consistently changed the trajectory for scaling IP networks.

The Nokia FP5 represents an evolutionary step forward in network processor (NP) silicon for high-performance routing. As the largest NP in the industry, it builds on the tremendous innovation pioneered by Nokia in the release of FP4 to integrate further, add additional capabilities and increase throughput and port speeds all while driving down power consumption significantly.

An NP-based architecture offers a completely programmable data path — one that can adapt to new features, functions and capabilities and scale with a simple microcode upgrade via a software download. It differs from fixed function ASICs, which have a hard-coded pipeline that cannot change, only via software wrappers. An NP offers the highest standard of network upgradability on the market, delivering the lowest TCO of any silicon architecture.

FP5 provides the foundation to drive the next generation of high-performance routers at the heart of tomorrow's networks. It does so while moving to next generation 800G interface speeds, increasing throughput to more than three times per line card and decreasing power over 75 percent compared to FP4 silicon. FP5 does this with line rate memories everywhere, best-in-class QoS and buffering, low latency and with a full IP/MPLS feature set that does not sacrifice capability.

IP networks are so essential to daily life that network security should not be an afterthought. Operators should not have to make sacrifices to add or enable network security. That's why line rate encryption and network security is built into FP5 with ANYsec. Network operators should equally have native tools to mitigate distributed denial of service (DDoS) attacks, making the network part of the solution for next-generation security. DDoS mitigation via signature-based access control lists (ACLs), using ACLs inspecting packet payloads, enables this. Where typical 5-tuple ACL-enabled systems complete DDoS attacks by filtering all traffic, FP5 offers the intelligence needed to truly filter good traffic from bad.

With FP5, Nokia delivers a new generation of high-performance routers that go beyond power reductions and speed enhancements to deliver capabilities and security above industry expectations and requirements. Service providers building and operating the world's most modern networks will benefit as FP5 charts a whole new route to the remarkable in IP networking.

Design requirements for today's IP networks

Unrelenting network growth is driving a new generation of platforms capable of rising to the challenge, but growth must go beyond size or capacity. A router should not have to get dumb to go fast; silicon capabilities matter. To that end, visibility and control, upgradability, backward compatibility, leading QoS capabilities and security must be additive to increased speed and throughput, generation over generation.

Operators continue to need visibility and control of their networks with a large number of statistics for all flow types, unicast traffic, multicast traffic, MPLS, segment routing and others. Scalability must continue to be high and multi-dimensional such that ACLs, MPLS, IP and MAC addresses can all scale concurrently. Trading off scale in one dimension for another is a recipe for compromise and constraining network growth over the long term.

At the same time, performance must be deterministic and predictable under all loading conditions. This can only be enabled using line rate memories everywhere for both buffering and tables.

The key driver for increasing network competitiveness and reducing recurring CAPEX is the flexibility to adapt to new networking standards. Modern routers must be designed not only to provide longevity in terms of their table growth and the ability to enable new performance features in hardware without a silicon upgrade, but also to mitigate against unknown future requirements such as SRv6 G-SID or slicing-ID.

Reducing energy costs is equally a top requirement for all network operators, and it is a fundamental tenet of FP5. FP5 capabilities such as intelligent aggregation and 800G optics support also contribute to ultra-low power consumption.

FP5 silicon is driven by and designed to address these critical design requirements for modern IP networks.

The power of silicon innovation

With FP5, Nokia demonstrates the power of silicon innovation through flexible capabilities, network security, scalable capacity and power efficiency. Through the years, Nokia has paved the way with an impressive set of industry firsts, and FP5 continues this legacy.

FP5 design leadership:

- At 6.0 Tb/s, the largest network processor (NPU) in the industry delivered with a 2.5D system-in-package (SiP) construct
- First NPU to support 112G SERDES, enabling a forward leap in energy efficiency and future generation optics support
- Largest device in the industry using line rate memories everywhere, for both buffering and tables, in a completely deterministic configuration
- First NPU with embedded line-rate network encryption for L2, L2.5 and L3
- First to support multiple 1.6 Tb/s clear channel flows

- First to support 800GE interface support, in high density, in a capacity-optimized configuration
- Only next-generation processor to support enhanced packet intelligence and control technology for a silicon-based approach to IP network security
- Only next-generation processor that does not compromise performance and functionality at the expense of capacity

FP5 silicon benefits:

- More than 3X capacity increase on the Nokia 7750 SR-s compared to Nokia FP4 silicon
- 75 percent reduction in power compared to Nokia FP4 silicon
- Ubiquitous, line-rate ANYsec encryption services without impacting performance
- Precise attack sensor and mitigation element for DDoS protection without impacting performance
- Highly programmable with zero hardcoded forwarding logic
- Integrated, fully buffered architecture with full ingress and egress buffering and line-rate memory
- Multi-dimensional scale for future growth, enabling concurrent scaling of all tables (L2, MPLS, IPv4/v6, ACLs)
- Support for 400G ZR/ZR+, 800G and 1.6 Tb/s speeds
- External MAC ASIC with QoS pre-processing, pre-classification, pre-buffering and first level DDoS protection and encryption

Flexible capability

Highly programmable

The NPU architecture of FP5 provides a fully programmable data path with no hardcoded forwarding logic. There are no special engines per logic core, and cores can be re-arranged in different configurations to add or enhance performance logic. This makes FP5 extremely adaptable and upgradable to future networking requirements.

G-SID compression for SRv6 and slicing-ID are two evolving network standards where a programmable pipeline can benefit. These functions can be enabled in hardware with a simple microcode upgrade via software download. As a result, this programmability offers the lowest TCO of any silicon on the market today.

Performance certainty

FP5 is deterministic across tables and buffering under all network loading conditions, which provides certainty at full scale and under real-world network conditions. This is enabled via integrated smart memories in the packet processor coupled with the fastest buffer memories in the industry. The FP5 memory set is best-in-class where other industry packet processors rely on non-line rate memories for buffering, for tables, or potentially for both. A line rate memory system will always outperform a non-line-rate memory system under all network loading conditions without exception. FP5 remains fully buffered with deep line rate ingress and egress buffers. Continuing to support full packet pre-classification and pre-buffering in front of the packet processor ensures a superior level of performance for all critical flows.

Backward compatible design

FP5 has been implemented to be fully backward compatible. FP4 and FP5 can be combined in the same chassis at the same time with line cards for both running at full line rate. Because full backwards compatibility is a key tenet of every generation of FP, FP5 provides full feature and scale interoperability with no interworking caveats.

When systems are upgraded to FP5, silicon and system design require no additional power or fan upgrades. All major FP4 investments can be fully preserved when migrating to enable higher capacity, throughput and port speed.

Intelligent aggregation

Intelligent aggregation allows any FP5-powered system to cost-effectively aggregate port capacity beyond the forwarding capacity of a delivered line card but continue to do this in a deterministic way with full respect for QoS and packet priority. Our most capable configuration for FP5 enables up to 19.2 Tb/s FD of intelligent aggregation. Many silicon alternatives on the market attempt to deliver on similar capabilities with non-line-rate memories and the illusion of full forwarding at line rate when memories are oversubscribed, but this is not the approach taken with FP5.

Intelligent aggregation allows for guaranteed QoS with full pre-buffering and pre-classification in front of our packet processor when used in an aggregation configuration. It enables an FP5-powered system to collapse full layers of pre-aggregation in front of systems or, if ports are constrained on an edge or core node, to expand the number of available ports without adding more line cards and continue to perform in a fully deterministic way under all network loading conditions. As a result, intelligent aggregation can be a significant driver of both CAPEX and OPEX savings.

Platform breadth and pay-as-you-grow licensing

19.2 Tb/s FD per line card is a tremendous amount of capacity and may not be required in all sites. Recognizing that networks need options not only to scale up but to scale down, we have implemented FP5 across a range of platforms and line card sizes from 2.4 Tb/s FD to 19.2 Tb/s FD.

Nokia offers a flexible pay-as-you-grow licensing model that provides a choice of entry points for immediate requirements and the ability to scale in-place for evolving needs with software-only upgrades. Operators can start with 800G or enable 800G ports later with a simple non-service impacting license. They can start with a stand-alone system at 9.6 Tb/s FD and grow it to 14.4 Tb/s FD or to 19.2 Tb/s FD when capacity requirements increase. With FP5, when an operator chooses reduced performance via a licensed approach, the result is not only the desired throughput but an equally proportional decrease in power consumption. FP5 has been designed with an adjustable core clock frequency to tune power to match performance.

The result is a system tailored to meet the exact performance, scale and feature requirements, with the right power profile and the right set of economics.

Speed and capacity

FP5 is the first ASIC on the market to deliver up to 48 ports of QSFP-DD 800 without further hardware or fabric upgrades. The economics behind 800G are trending to be on-par with two 400G optics — but the 800G optics will save between 25 and 43 percent of the power budget of 400G. As systems become denser, the power associated with optics alone becomes a significantly larger portion of total power consumption. 800G optics support changes the game relative to 400G.

FP5 supports standardized FlexE 2.0 for "super-rating" — the ability to bond multiple 100GE, 200GE and 400GE interfaces into a combined 1.6Tb/s clear channel flow today, well in advance of standardized 1.6T optics. Super-rating enables full use of all bandwidth in a bundle without the inefficiencies of hashing or link aggregation groups (LAGs), greatly simplifying network topologies. In addition, Nokia FlexE 2.0 bundles still support full QoS at up to 1.6 Tb/s clear-channel speeds with bundle redundancy and service flexibility.

800G optics and 1.6 Tb/s flow support clearly demonstrates the forward-looking ability of FP5 to accommodate future network speeds.

Network security

ANYsec line-rate encryption

Network security can no longer be an afterthought in IP network design and deployment. Operators must move toward a holistic approach to end-to-end network security, avoiding trade-offs with piecemeal MACsec or IPsec solutions. Enabled by FP5 silicon, ANYsec provides universal, low-latency, line-rate encryption for L2, L2.5 and L3. ANYsec can be applied to any transport, at any speed (10 Gb/s, 25 Gb/s, 100 Gb/s, 200 Gb/s, 400 Gb/s, 800 Gb/s, 1.6 Tb/s) and is supported on any FP5-based line card connector. It goes beyond MACsec support to provide MPLS- and IP-level line rate encryption in a service-oriented way that can be delivered either hop by hop or end to end as a security overlay. It is fully interoperable with all legacy equipment in a network, allowing for secure transport via any FP5-to-FP5 path.

ANYsec is service oriented: it runs over MPLS, segment routing, Ethernet virtual private network (EVPN), Border Gateway Protocol (BGP) and any Interior Gateway Protocol (IGP). As such, it offers a true unifying capability to not only secure internal links within a network against bad actors or man-in-the-middle attacks but enables new services and revenue generation for the secure transport of sensitive or mission-critical data.

Multi-level DDoS mitigation

To identify and neutralize DDoS attacks automatically, FP5-based 7750 SR routers can be combined with the software analytics of Nokia Deepfield Defender. Security policies are continuously monitored and tuned using Nokia Service Router Operating System (SR OS) telemetry from the 7750 SR. With automated workflows in Deepfield Defender, tens of thousands of FP5 filters are updated in seconds to respond to changing security conditions without delay. The filters associated with DDoS mitigation are signature ACLs. Signature-based ACLs go beyond typical 5-tuple ACLs that complete DDoS attacks by impacting all traffic. Instead, they provide payload-level inspection capabilities at line rate to truly filter out DDoS traffic.

Advanced control plane protection

The real world has microbursts, threat attacks and packet storms, none of which can be allowed to compromise the IP router control plane. FP5-based router line cards implement pre-buffering and pre-classification (with priority tagging) in the dedicated MAC chip to guarantee the availability and protection

of the control plane. In addition, Nokia FP-based routers leverage FP silicon in the router control card to enable a centralized rate-limiting function on traffic destined for the control plane CPU.

Power efficiency

With the rise in popularity of non-line-rate systems, many operators believe that to be power efficient, a system must sacrifice capability. In other words, the system must get dumb to go fast. The fallacy is that performance, statistics, network visibility, buffering, QoS and deterministic performance must all be sacrificed to save power while concurrently increasing throughput.

FP5 changes the game. Delivering typical power consumption on the order of 0.1W/Gig, full featured, with line rate memories everywhere and full buffering via a completely upgradable NPU architecture, FP5 systems deliver the same order of power consumption as lean-core and merchant silicon systems — but with no trade-offs.

FP5 takes a holistic approach to silicon and router design. By avoiding the re-use of datacenter-specific chassis designs, the mechanical design used to realize FP5 provides best-in-class cooling with no air turns, using hexagonal mesh air intakes which are 90 percent open. Power density optimization, 112G SERDES and chipset consolidation within the FP5 disaggregated chipset architecture also drive power savings. Together, these design considerations provide a 75 percent power reduction generation-over-generation. System upgrades to FP5 require no power infrastructure changes as a fully loaded FP5 system fits within the same power envelope as the same FP4 fully loaded system.

Power consumption and sustainability are top of mind for every network operator. The energy-efficient design of FP5-based 7750 SR systems increases the sustainability of IP networks through reduced emissions.

Summary

IP networks of the future must be designed to accommodate the unexpected. Recognizing this reality, Nokia FP5 silicon delivers powerful silicon innovation through flexible capabilities, network security, scalable capacity and power efficiency. With systems and line cards that scale from 2.4 Tb/s FD to 18 Tb/s FD and up to 19.2 Tb/s FD with intelligent aggregation, and flexible licensing options, FP5 delivers a full breadth of systems and sizes to tune to exact network requirements. We are first to market with 800G optics in high density, enabling significant power savings over 400G and reducing optical power consumption.

FP5 is fully programmable with line rate memories everywhere for both tables and buffers. FP5 is designed to be deterministic, providing certainty under all loading conditions. This is the case across ACLs, services and at all scaling levels.

A no-compromise design approach has been taken at every step in the evolution of FP5. As a result, all the above capabilities are implemented with full-featured power consumption of 0.1W/Gig.

With the FP5, we are confirming our focus on delivering innovative, core technologies that provide our customers with the right foundation for the future. That foundation addresses the challenges we know, such as the need to deliver more bandwidth more efficiently for increasingly complex and demanding network services, but also the challenges we can't predict, by delivering future-proof silicon that charts a whole new route to the remarkable in IP networking.

About Nokia

At Nokia, we create technology that helps the world act together.

As a B2B technology innovation leader, we are pioneering the future where networks meet cloud to realize the full potential of digital in every industry.

Through networks that sense, think and act, we work with our customers and partners to create the digital services and applications of the future.

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